IN THE CLAIMS

Claims 1-22 (Cancelled)

23. (Previously presented) A processing device, comprising:

a reconfigurable circuit allowing change in function;

a first path portion transmitting an output of said reconfigurable circuit as an input to said reconfigurable circuit;

a setting portion supplying setting data for configuring an intended circuit in said reconfigurable circuit; and

a control portion controlling said setting portion such that a plurality of setting data are successively supplied to said reconfigurable circuit, so that an output of a circuit configured on said reconfigurable circuit in accordance with one setting data is supplied to an input of a circuit configured in accordance with next setting data through said first path portion; and

an internal state holding circuit receiving an output of said reconfigurable circuit,

said internal state holding circuit being connected to said first path portion;

said device further comprising:

a memory portion storing in a prescribed area an output of a circuit configured on said reconfigurable circuit in accordance with said one setting data; and

a second path portion transmitting the output of the circuit configured on said reconfigurable circuit stored in said prescribed area of said memory portion as an input to a circuit configured in accordance with the next setting data.

24. (Previously presented) The processing device according to claim 23, wherein said internal state holding circuit operates at a higher speed than said memory portion.

25. (Previously presented) The processing device according to claim 23, wherein said setting portion successively supplies a plurality of setting data to said reconfigurable circuit, so that one circuit is formed as a whole.

26. (Previously presented) The processing device according to claim 23, wherein said plurality of setting data represent a plurality of divided circuits obtained by dividing one circuit.

27. (Previously presented) The processing device according to claim 23, wherein said reconfigurable circuit is configured as a combinational circuit.

28. (Previously presented) The processing device according to claim 23, further comprising:

an output circuit receiving an output of said reconfigurable circuit,

said output circuit providing the output of said reconfigurable circuit when said reconfigurable circuit is configured a plurality of times by said setting portion.

29. (Previously presented) The processing circuit according to claim 23, further comprising:

a switching circuit switching between the input from said second path portion and an external input, to be an input to said reconfigurable circuit.

30. (Currently amended) The processing device according to claim 23, wherein

said reconfigurable circuit includes a plurality of logic circuits each capable of selectively executing a plurality of operation functions, and a connecting portion allowing setting of a connection relation among the logic circuits; and

said setting portion sets the functions and said connection relation of said logic circuits.

31. (Previously presented) The processing device according to claim 30, wherein

said logic circuit is an arithmetic logic circuit capable of selectively executing a plurality of multi-bit operations.

Claims 32 and 33 (Cancelled)

34. (Previously presented) A processing device, comprising:

a reconfigurable circuit allowing change in function and connection relation;

a setting portion storing setting data representing a divided unit forming a part of an intended circuit and supplying the setting data to said reconfigurable circuit; and

a control portion controlling said setting portion such that a plurality of setting data are successively supplied to said reconfigurable circuit to configure said intended circuit; wherein

said reconfigurable circuit has at least one state holding circuit holding an internal state;

said reconfigurable circuit is divided, by an arrangement of said state holding circuit, into a plurality of stages of reconfigurable units; and

said control portion controls said setting portion such that when a plurality of intended circuits are to be configured, setting data for configuring divided units each forming a part of the

circuits on respective ones of said plurality of stages of reconfigurable units are successively supplied along a process flow.

35. (Currently amended) The processing device according to claim 34, wherein

said reconfigurable circuit is divided, by an arrangement of N state holding circuit, into (N+1) stages of reconfigurable units;

said control portion controls said setting portion such that at one time point, setting data of a divided unit configuring an intended circuit is supplied to a ~~said~~ reconfigurable unit between i-th state holding circuit and (i+1)th state holding circuit,

controls said setting portion such that at a next time point, setting data of a next divided unit configuring said intended circuit is supplied to said reconfigurable unit between (i+1)th state holding circuit and (i+2)th state holding circuit in accordance with the process flow, and controls said setting portion such that setting data of a divided unit configuring a different intended circuit is supplied to said reconfigurable unit between i-th state holding circuit and (i+1)th state holding circuit.

36. (Currently amended) The processing device according to claim 34, wherein

said reconfigurable circuit is divided, by the arrangement of N state holding circuits, into N stages of reconfigurable units;

said control portion controls said setting portion such that at one time point, setting data of a divided unit configuring an intended circuit is supplied to a ~~said~~ reconfigurable unit between i-th state holding circuit and (i+1)th state holding circuit,

controls said setting portion such that at a next time point, setting data of a next divided unit configuring said intended circuit is supplied to said reconfigurable unit between (i+1)th state

holding circuit and (i+2)th state holding circuit in accordance with the process flow, and controls said setting portion such that setting data of a divided unit configuring a different intended circuit is supplied to said reconfigurable unit between i-th state holding circuit and (i+1)th state holding circuit;

said device further comprising

a path portion for providing an input from the N-th state holding circuit ~~portion~~ to the first stage of reconfigurable units.

37. (Currently amended) The processing device according to claim 34, wherein

a ~~said~~ reconfigurable unit is configured as a combinational circuit.

38. (Previously presented) The processing device according to claim 34, further comprising:

an output circuit receiving an output of said reconfigurable circuit,

said output circuit providing the output of said reconfigurable circuit when said reconfigurable circuit is configured a plurality of times by said setting portion.

39. (Previously presented) The processing circuit according to claim 34, further comprising:

an internal state holding circuit receiving an output of said reconfigurable circuit; and

a first path portion inputting the output signal held by said internal state holding circuit to the first stage of reconfigurable units.

40. (Previously presented) The processing device according to claim 39, further comprising:

a memory portion storing in a prescribed area an output of said reconfigurable circuit in accordance with a setting data; and

a second path portion transmitting the output of the circuit configured on said reconfigurable circuit stored in said prescribed area of said memory portion as an input to a circuit configured in accordance with the next setting data.

41. (Previously presented) The processing circuit according to claim 40, further comprising:

a switching circuit switching between the input from said second path portion and an external input, to be an input to said reconfigurable circuit.

42. (Currently amended) The processing device according to claim 34, wherein

a ~~said~~ reconfigurable unit includes a plurality of logic circuits each capable of selectively executing a plurality of operation functions, and a connecting portion allowing setting of connection relation among the logic circuits; and

said setting portion sets the functions and said connection relation of said logic circuits.

43. (Previously presented) The processing device according to claim 42, wherein

said logic circuit is an arithmetic logic circuit capable of selectively executing a plurality of multi-bit operations.